HSSub™

A Single Integrated Solution for Defense & Aerospace Bus Test Appications

The Teradyne High Speed Subsystem (HSSub) is a powerful and flexible solution for current, emerging, and future bus test requirements for weapon system assemblies. HSSub augments new and existing factory, field, and depot test systems, addressing the latest high-speed serial technologies as well as legacy buses. As multi-gigabit buses, high-level protocols, and optical networking become dominant, HSSub will continue to provide cost benefits for acquisition, test generation, and long-term sustainment through the advantages of a unique architecture and highly configurable instrumentation.

The Challenge of Evolving Bus Test Requirements

The interconnections between weapon system assemblies are evolving from wide parallel buses to increasingly faster, narrower, and more standardized serial buses. Electrical signaling is moving from single-ended to faster differential approaches, and to optical transmission for increased speed and reliability. Bus bandwidth continues to grow along with increasingly complex data and protocols riding on top of them. Test systems must provide long-term solutions for multiple generations of assemblies that present this entire range of requirements.

The ad hoc and diverse nature of older bus designs demands instruments with great programming flexibility. The standardization and performance of newer buses is facilitating higher level applications that create new test challenges. Testing is becoming less about the exchange of raw data, and more about Upper Level Protocols associated with inter-assembly control and exchange of images, video, or sensor/transducer data. Instruments must be capable of real-time movement and processing this data. As this bus evolution takes place, test strategies move from the traditional bit and register level to interacting with large quantities of data with complex procedures. ATE must address an increasing quantity of ports, types, concurrency, and Upper Level Protocols with buses of all ages, sometimes mixed on the same UUT.

The Inadequacies of Current Bus Test Approaches

Over the last two decades, ATE deficiencies have forced test engineers to employ TPS-specific instruments or fully custom ITA-based circuitry. The result is high long-term logistics costs due to early obsolescence, lack of flexibility, low throughput, and inadequate documentation and applications support.

Specialized bus instruments and design verification equipment is not well-suited to automated systems because they generally lack conformance to ATE hardware and software standards, as well as providing a limited product lifetime. Custom ITA circuitry may deliver nominal functionality, but it typically performs as a black box, understood by few, and lacking the flexibility and support resources required for efficient test development and support.

Configurable FPGA-based instruments are increasingly considered as a potential alternative to TPS-specific instruments or

Key Features

- **Configurable, high-performance instrumentation:** Serial or parallel buses, electrical or optical, standardized or custom, new or legacy, all speeds
- **Reusable HSSub Apps:** Rapidly configure Runtime Defined Instruments and provide UUT-centric TPS programming
- **Three Tier Architecture:** Open and standards-based integration of programmable hardware, real-time processing, and Windows technology
- **Optical Power Management and Switching:** Integration of HSSub and Teradyne VERTA Instrumentation for critical parametric optical test

Advantages & Benefits

- **Superior performance and programming efficiency** results in the lowest TPS development cost
- **High throughput** results in the lowest labor and equipment cost
- **Flexible, sustainable, well-supported products from a proven supplier** results in the lowest long-term integration and logistics cost
- **The combination** results in the lowest overall life-cycle cost of ownership

fully custom ITA-based circuitry. However, most approaches lack a structured methodology for system integration, TPS development, reusable bus protocol support, and coordination of multiple instruments. Most configurable instruments are overly focused on low-level bus requirements, leaving the TPS Engineer with few resources and tools to provide the upper-level functionality, which often requires real-time operation. A UUT that communicates video needs an instrument that operates at that level with a single high-level TPS function call, not one where the developer is forced to encode and decode millions of pixels.

The Superior HSSub Bus Test Architecture

HSSub avoids the inefficiencies of conventional approaches with a powerful combination of coordinated, reconfigurable, multi-purpose instruments. HSSub is a PXI Express subsystem that can augment an existing system, form the nucleus of a new large-scale test system, or serve as a self-sufficient bench-top tester. HSSub can consist of a single instrument, or a large, multiple chassis solution.

HSSub instruments employing high-performance FPGAs, processors, and programmable devices are configured and combined to satisfy real-time UUT-specific requirements. The Windows computer provides supervision, setup, as well as preparation and analysis of runtime test data. These functional layers form the HSSub Three Tier Architecture, consisting of low-level I/O Protocol Processing (tier 1), upper-level Real-Time Computing (tier 2), and Windows-based Resource Management (tier 3).

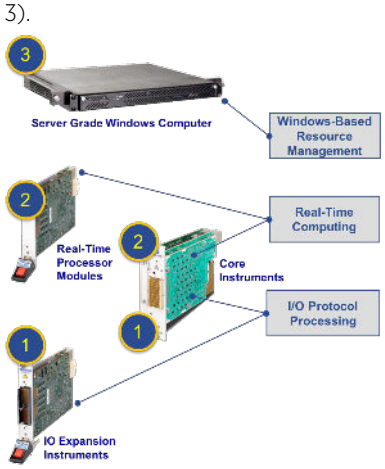

Figure 1: HSSub Three Tier Architecture

This arrangement places time-critical protocol functionality within the instruments, leaving the multi-tasking Windows computer to concentrate on pre-test setup and post-test analysis. By avoiding real-time bottlenecks HSSub is scalable; additional concurrent buses are supported by adding more smart instruments.

Unlike the isolated capabilities of individual instruments, HSSub TriFlexTM infrastructure software simplifies activities across the subsystem; from integration with the test system, coordination between instruments, building of reusable application-specific solutions, and most importantly, streamlining TPS development.

The HSSub architecture facilitates programming at the level of abstraction dictated by the UUT. This may entail interactions ranging from low-level bit, register or data packet transactions to high-level video stream or complex control operations. HSSub has tiers of functionality that address the Lower Level Protocols of each bus, the Upper Level Protocols that operate on top of them, and Windows-based TPS programming. HSSub excels at flexible low-level bus capabilities, either alone, or in combination with the increasingly important high-level protocols. The HSSub software that embodies this functionality and provides a familiar TPS application programming interface (API) is called an HSSub App.

Reusable Application-Specific HSSub App Solutions

For all programming tasks, the TPS invokes an application-specific HSSub App that rapidly configures one or more Runtime Defined Instruments and provides a Windows TPS programming interface just like an instrument driver on the subsystem computer. The reusable HSSub App provides the TPS with the appropriate level of functionality while encapsulating the necessary bus protocol implementation.

HSSub Apps are distributed and deployed as a single file that contains the components for a specific application. First, an HSSub App is invoked by a TPS, and the Configuration Data loads FPGAs, initializes chipsets, and provides processor code for one or more instruments. Next, the App Interface provides an IVI-like C/C++/C# API with the same functionality and methodology as a dedicated instrument driver. Unlike conventional single-purpose instruments, HSSub instruments take on any number of roles by association with multiple HSSub Apps. Programming takes place at the appropriate level of abstraction, dictated by specific UUT requirements. While many HSSub Apps provide Upper Level Protocol support using all three tiers, others focus on low-level bus functionality, bypassing tier 2 when it is not required.

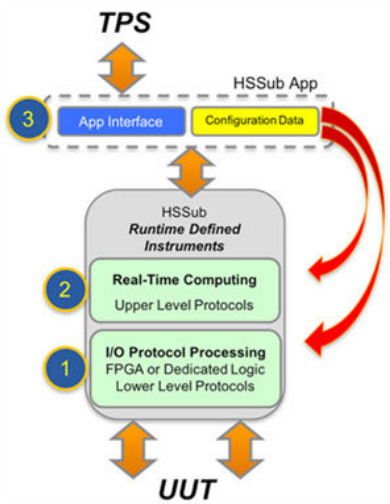

Figure 2: HSSub App *Configuration Data* and *App Interface*

Most HSSub Apps are provided to TPS developers, they usually don't need to develop them. Subject matter experts at Teradyne, third-parties, and end users create HSSub Apps using open development methodology and conventional software tools. Teradyne supplies a broad range of HSSub Apps that address various low-level buses and Upper Level Protocols. End-user and third-party developers can develop their own HSSub Apps, often adapting existing proprietary weapon system design data expressed in standard languages such as VHDL/Verilog and C/C++/C#. The HSSub TriFlexTM software includes sample projects, code libraries, and development tools for the creation, packaging, and distribution of user-created reusable HSSub Apps.

Teradyne offers a wide range of HSSub Apps with low-level bus support ranging from high port count RS232, Ethernet, Fibre Channel, and multigigabit serial with optical I/O. High-level protocol support includes network services such as FTP/TFTP/DHCP, video over various buses, UUT configuration

downloading, and inter-assembly data transfer.

Flexible Integration in HSSub Foundations

Figure 3: HSSub Foundation

HSSub Foundations provide a PXI Express 3U chassis, a 64-bit Windows-based computer, and the TriFlexTM infrastructure software. A family of available Foundations support internal and ancillary system integration, or standalone table-top use. Foundation capacities range from 3 to 17 instrument slots, and multiple chassis can be combined for additional capability.

HSSub is controlled by a powerful embedded PXI computer or an external server-grade computer, capable of running an entire test system. When integrating into an existing test system, the HSSub interfaces via Ethernet as an LXI instrument. The HSSub Computer and the **TriFlex™** software manage control and data flow of the HSSub Instruments. Foundations are populated with HSSub instruments, as well as third party instruments.

Flexible Physical Interface Options

HSSub physical interface options support a broad range of mechanical system configurations. Systems that already have a suitable UUT interface approach can use Direct-to-Instrument interfacing.

Figure 4: Front Panel Instrument Interface

HSSub instruments employ high-density, high-performance front panel connectors that accept cabling to the mechanical interface. Teradyne recommends the connectors and cabling that are appropriate for the various bus types, and can provide custom design and fabrication services, if required.

Many systems do not have an existing, technically acceptable interface approach, and the HSSub Mass Interconnect approach is a common solution. The combination of HSSub instruments and unique funnel modules support both Virginia Panel G20 ITAs and i2 MX cabled connections.

Figure 5: Funnel Instrument Interface

The cable approach is appropriate when there is a simple bus relationship from instrument to UUT connectors. An ITA is appropriate for cases where buses in multiple instruments buses are distributed to multiple UUT connectors in a more complex manner.

Figure 6: Cable or ITA Interface

HSSub Advantages and Benefits

HSSub is optimized for programming efficiency. HSSub Apps are efficient solutions that are reusable across multiple test programs, developers, and organizations. TPS programming targets the level of detail dictated by the UUT. HSSub employs conventional languages understood by Test, Design, and TPS maintenance personnel. HSSub provides uniform implementation, documentation, and training across all products. These HSSub advantages provide the benefit of lower programming costs.

HSSub is optimized for high throughput, efficiently transferring and processing the ever-increasing quantities of test data flowing throughout the subsystem. Concurrent bus operation minimizes execution time. Complex operations take place in the appropriate location, either within the instruments or the central computer. HSSub shortens test and wait times to increase programming and production personnel productivity while minimizing hardware requirements. These HSSub advantages provide the benefit of lower labor and equipment costs.

HSSub is optimized for long-term sustainment. Teradyne a supplier with decades of success supporting equipment used in Defense & Aerospace test and HSSub design, manufacturing, and support leverages that experience. HSSub Architectural flexibility avoids the crippling expense of equipment obsolescence by the ability to address new or changing requirements and minimizing the overall quantity of instrumentation equipment requirements. These HSSub advantages provide the benefit of lower cost of long-term sustainment.

HSSub alternatives are typically combinations of complex ITA circuitry, single purpose bus instruments, and basic configurable instruments. The complexity of multi-source approach complicates integration, training, and TPS development. The combination is rarely optimized for runtime efficiency, TPS sustainment, or equipment maintenance. HSSub provides a series of advantages including superior performance, integration, extensibility, consistency, long-term technical and logistics support, and a supplier with a proven Defense & Aerospace track record. These HSSub advantages provide the benefit of lower overall cost of ownership.

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The HSSub Family of Instruments

The extensive capabilities and flexibility of the HSSub instrument family is ideal for addressing the full range of system requirements and configurations, with variables such as:

- Location at factory, field, or depot
- Any quantity of buses and bus types
- Standard or custom protocols
- The latest fast serial buses, older legacy designs, or combinations of both

The instruments all share common hardware design principles such as high bandwidth data paths, large and fast memories, configurability, and local real-time processing where appropriate. All instruments are programmed using application-specific HSSub App solutions, and the overall system is integrated with the TriFlexTM infrastructure software. The HSSub instruments are grouped into several categories based on the various roles that they provide.

Reconfigurable Core Instruments combine a Test Defined FPGA for low-level (tier 1) high-performance bus configurability, and a discrete multi-core processor and the VxWorks RTOS for flexible high-level protocol (tier 2) support. The LVDS Core Instrument provides direct I/O for 64 differential data pairs and the Serial Core Instrument provides 16 Multi-Gigabit Transceivers. These instruments are ideal when Upper Level Protocols for applications such as video or data exchange operate on top of standardized Lower Level Protocols such as Fibre Channel.

The ***RT Processor Module*** provides Upper Level Protocol (tier 2) support with real-time capabilities identical and compatible with that of the Core Instruments. Typically, these modules are associated in software with another instrument that provides low-level (tier 1) bus support.

Reconfigurable Core Instruments combine a Test Defined FPGA for low-level (tier 1) high-performance bus configurability, and a discrete multi-core processor and the VxWorks RTOS for flexible high-level protocol (tier 2) support. The HSSub-5010 Reconfigurable LVDS Core Instrument provides direct I/O for 64 differential data pairs and the HSSub-5050 Reconfigurable Serial Core Instrument provides 16 Multi-Gigabit Transceivers. These instruments are ideal when Upper Level Protocols for applications such as video or data exchange operate on top of standardized Lower Level Protocols such as Fibre Channel.

The HSSub-5020 ***Real-Time Processor Module*** provides Upper Level Protocol (tier 2) support with real-time capabilities identical and compatible with that of the Core Instruments. Typically, these modules are associated in software with another instrument that provides low-level (tier 1) bus support.

Reconfigurable IO Expansion Instruments (IOXI) address a wide range of requirements from legacy to the latest multi-gigabit buses with powerful Test Defined FPGAs and tightly integrated memory for low level (tier 1) support. Instruments provide specialized signaling such as Low Voltage TTL (LVTTL), Multi-Point LVDS (M-LVDS), and optical transmission. When Real-Time Computing (tier 2) is required, instruments are associated in software with any available HSSub RT Processor, otherwise they may be directly controlled by the HSSub Windows computer.

The IOXI instruments include:

- HSSub-6020 Reconfigurable LVTTL
- HSSub-6040 Reconfigurable Hybrid
- eDigital-6020A Reconfigurable Essential Digital
- HSSub-6100 12G Reconfigurable

Flexible IO Expansion Instruments (FIOXI) combine a common reconfigurable Test Defined FPGA backbone with two bus-specific Physical Interface Modules (PIMs) that reduce or eliminate the need for external interface circuitry. Teradyne rapidly develops PIMs that are integrated in various combinations. Current PIM capabilities include RS485 (32 pairs), RS232 (up to 36 ports)/IRIG-B, HOTLink/ECL, and 1G Ethernet.

The FIOXI instruments include:

- HSSub-9030 RS485/HOTLink/ECL
- HSSub-9050 RS232/IRIG-B/Ethernet
- HSSub-9080 RS485/RS232/IRIG-B
- HSSub-9100 RS485 (64 pair)
- HSSub-9110 RS232/IRIG-B/HOTLink/ECL

Standard Bus Instruments

The HSSub Standard Bus Instruments support common, highly standardized serial buses with the greatest performance and density available in the 3U PXI Express form factor by using the latest, highly integrated chipsets.

The Standard Bus Instruments include:

- HSSub-6090 1G Ethernet
- HSSub-6091 10G Ethernet
- HSSub-6120 AS5643 Mil-FireWire
- HSSub-8030 Peripheral Bus

Additional Instruments and Accessories provide conversion between instruments with electrical I/O and optical UUT ports. The HSSub Remote Test Head is a small chassis that can house up to four HSSub instruments, located away from the main HSSub Foundation for applications such as testing in an environmental test chamber.

The Additional Instruments include:

- HSSub-6065 4-Channel Optical IO Expansion Instrument
- HSSub-7050 Remote Test Head
- VERTA Optical Power Management and Switching Instrumentation

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