FURUNO

Multi-GNSS Disciplined Oscillator

GF-8801, GF-8802, GF-8803
GF-8804, GF-8805

User's Guide

(Document No. SE22-900-005-01)

FURUNO ELECTRIC CO., LTD.

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IMPORTANT NOTICE

In this product, FURUNO can ensure safe performance only the commands and the sentences which are written in this document or are written in the document for this product. Please do not use the commands of the others products, otherwise this product may have troubles and FURUNO may not support about the troubles.

The following satellite systems are operated and controlled by the authorities of each government.
- GPS (USA)
- GLONASS (Russia)
- Galileo (Europe)
- QZSS (Japan)
- SBAS (USA: WAAS, Europe: EGNOS, Japan: MSAS, India: GAGAN)

Thus FURUNO is not liable for the degradation of the above systems so therefore FURUNO cannot guarantee specification based on their conditions. By solar flare or coronal mass ejection due to solar surface activity, depending on the scale, there is a possibility that a decrease in reception sensitivity or deterioration in precision may be temporarily observed. User is expected to be familiar with the System and make full use of it with their own responsibility.

Revision History

No.	Contents	Date
0	First Release	2022.04.07
1	Correct section 3.3	2022.10.06

Table of Contents

1 Outline

This document describes the essential information for achieving proper operation and performance of the following FURUNO Multi-GNSS Disciplined Oscillator (GNSSDO) solutions. It is a guide for user development, design, manufacturing and quality control.
Products: GF-880x series (GF-8801, GF-8802, GF-8803, GF-8804 and GF-8805)

2 General Functional Block Level Diagram

This chapter describes main functions of the GNSSDO. Figure 2.1 shows an example block level diagram of the GNSSDO. The GNSSDO has the following two kinds of PPS;

- Reference PPS: This PPS is synchronized with UTC using the GNSS receiver or with an external 1Hz signal (EPPS).
- Local PPS: This PPS is a signal divided from 10MHz which is controlled by PLL.

The GNSSDO operates the adaptive feedback control with two PPS signals as an output PPS source. The GNSSDO is able to achieve a high precision holdover by means of the adaptive control regarding voltage of Oscillator.

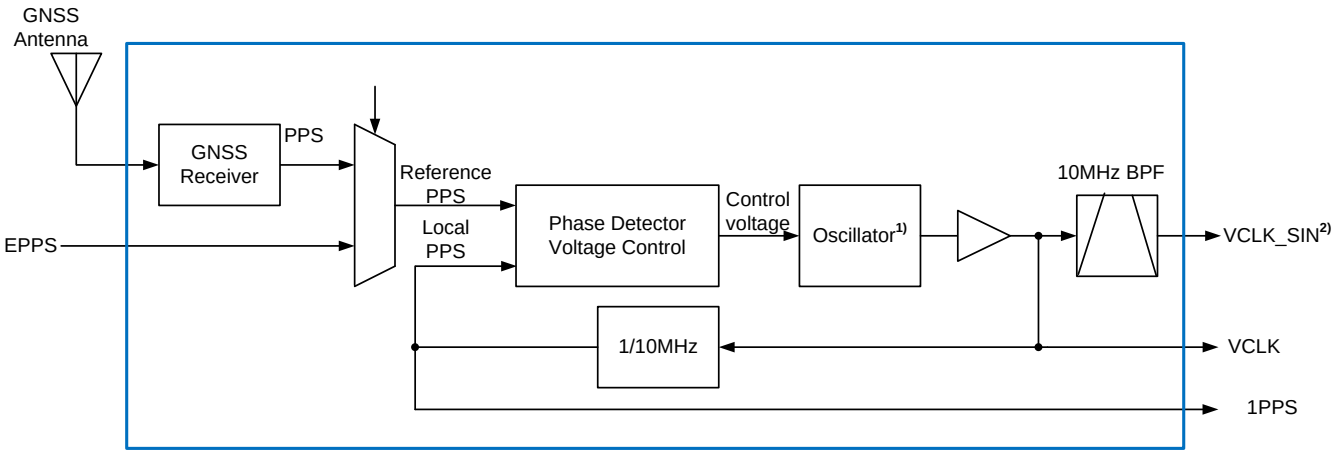

Figure 2.1 GF-880x General Block Level Diagram

Notes:
(*1) GF-8801:VTCXO, GF-8802/03/04/05: OCXO
(*2) GF-8801, GF-8802 and GF-8803 do not support VCLK_SIN.

3 General Performance Data

This chapter describes each signal of the specification and typical test data values in order to check the consistency between the product specifications and customer requirement specifications.

3.1 PPS

Table 3.1 shows the specifications and the actual values of PPS at Holdover.

Table 3.1 PPS Performance Specifications and Test Data

			GF-880x series				
Item	**Receiver status**	**Holdover condition**	**8801**	**8802**	**8803**	**8804**	**8805**
Time Precision(1)	Fine Lock	-	±4.5 ns (at 1σ)				
	Holdover	-	-				
Time accuracy(1)	Fine Lock	−	±40ns (at UTC)				
	Holdover（within 24 hours）		-	±50us	±10us	±5us	±1.5us
	Holdover（within 1 hours）		-	±3us	±3us	±400nsec	±400nsec

-: Not Applicable

Notes:
(*1) Refer to Section 4.1 of the Hardware specifications for environmental conditions.

3.2 VCLK

Table 3.2 shows an overview of VCLK specifications. There is no definition of frequency precision because the short term stability of VCLK defines the same stability specifications noted in this table. The phase noise of 10MHz at GF-8801/02/03 is actual value test data. Therefore there is no description of this value in hardware specifications. User can check the performance using test data in Figure 3.1, Figure 3.2 and Figure 3.3. The phase noise of 10MHz at GF-8804 and GF-8805 is described as performance specifications in the hardware specifications. To guarantee the performance specification, the phase noise exceeding 10kHz is specified the same as 1kHz (-140dBc/Hz). However the actual value of phase noise exceeding 10kHz is better than 1kHz. User can check the performance using test data in Figure 3.4.

Table 3.2 VCLK Performance Specifications

Item		Receiver status	Unit	GF-880x series				
				8801	8802	8803	8804	8805
Short term stability(1) (Root Allan deviation τ=1sec)		Fine Lock	-	±5E-10 (Max)	±5E-11 (Max)	±2E-11 (Max)	±1E-11 (Max)	
		Holdover						
Long term stability (1) (Average 24 hour)		Fine Lock	-	±1E-11 (Max)	±1E-12 (Max)			
		Holdover	-	-	±1E-9 (Max)	±2E-10 (Max)	±1E-10 (Max)	±3E-11 (Max)
10MHz Phase noise	1Hz	Fine Lock	dBc/Hz	-70 (Typ)	-75 (Typ)	-85 (Typ)	-85 (Max)	
	10Hz			-100 (Typ)	-106 (Typ)	-110 (Typ)	-120 (Max)	
	100Hz			-122 (Typ)	-134 (Typ)	-135 (Typ)	-130 (Max)	
	1kHz			-141 (Typ)	-146 (Typ)	-148 (Typ)	-140 (Max)	
	>10kHz			-148 (Typ)	-149 (Typ)	-155 (Typ)	-140 (Max)	
	1Hz	Holdover		-70 (Typ)	-75 (Typ)	-85 (Typ)	-85 (Max)	
	10Hz			-100 (Typ)	-106 (Typ)	-110 (Typ)	-120 (Max)	
	100Hz			-122 (Typ)	-134 (Typ)	-135 (Typ)	-130 (Max)	
	1kHz			-141 (Typ)	-146 (Typ)	-148 (Typ)	-140 (Max)	
	>10kHz			-148 (Typ)	-149 (Typ)	-155 (Typ)	-140 (Max)	
Accumulating phase noise	10 to 10kHz	Fine Lock	dBc	-	-	-	-95 (Max)	
		Holdover		-	-	-		

-: Not Applicable

Notes:
(*1) Refer to Section 4.1 of the Hardware specifications for environmental conditions.

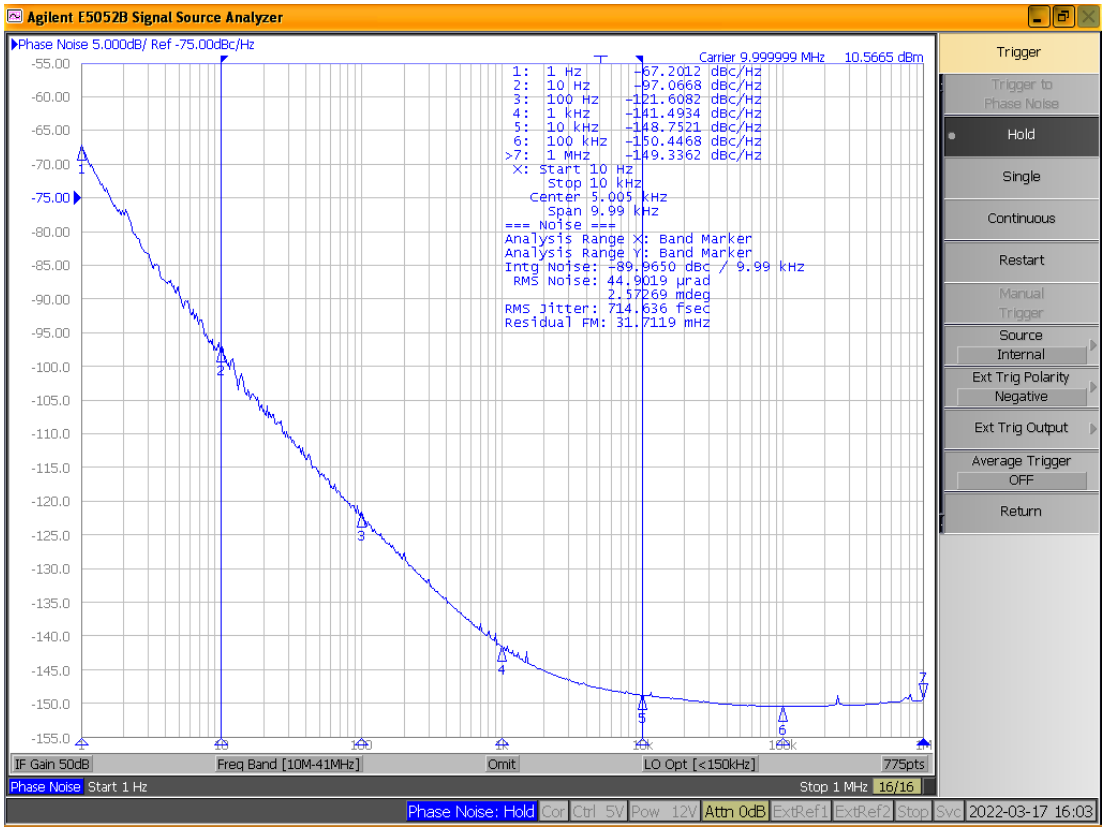

Figure 3.1 VCLK Phase Noise Data (GF-8801)

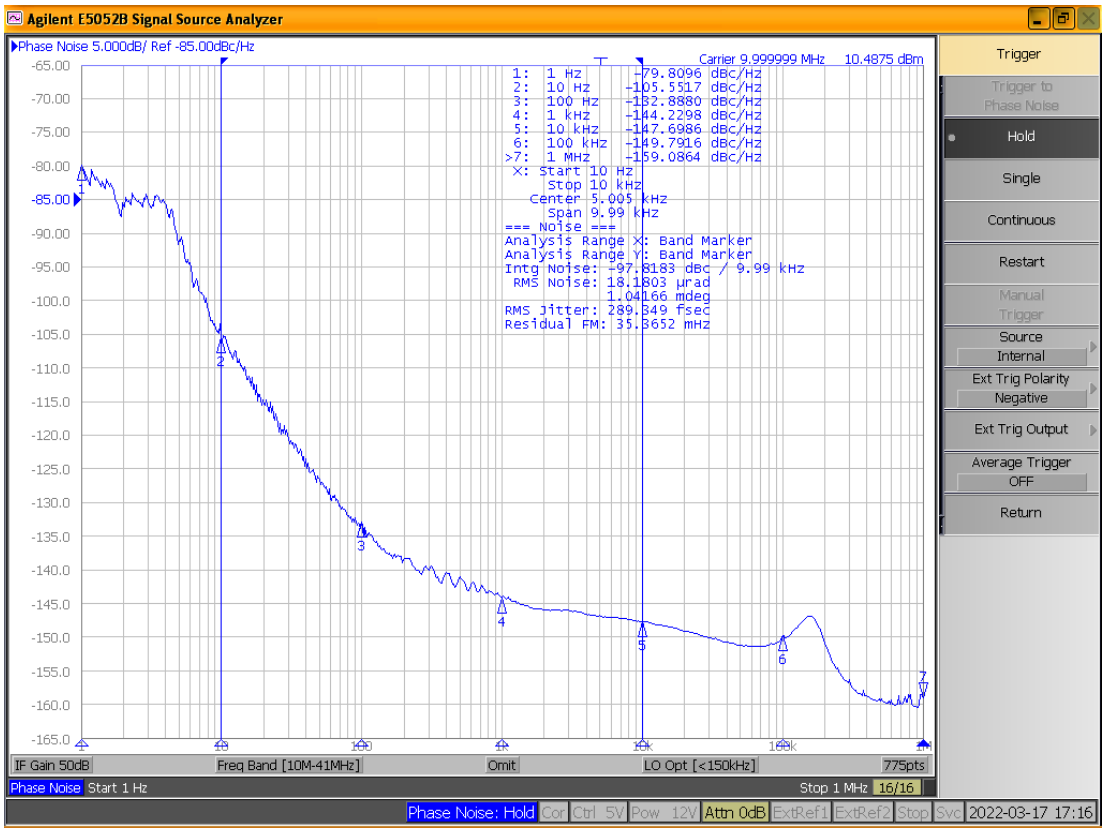

Figure 3.2 VCLK Phase Noise Data (GF-8802)

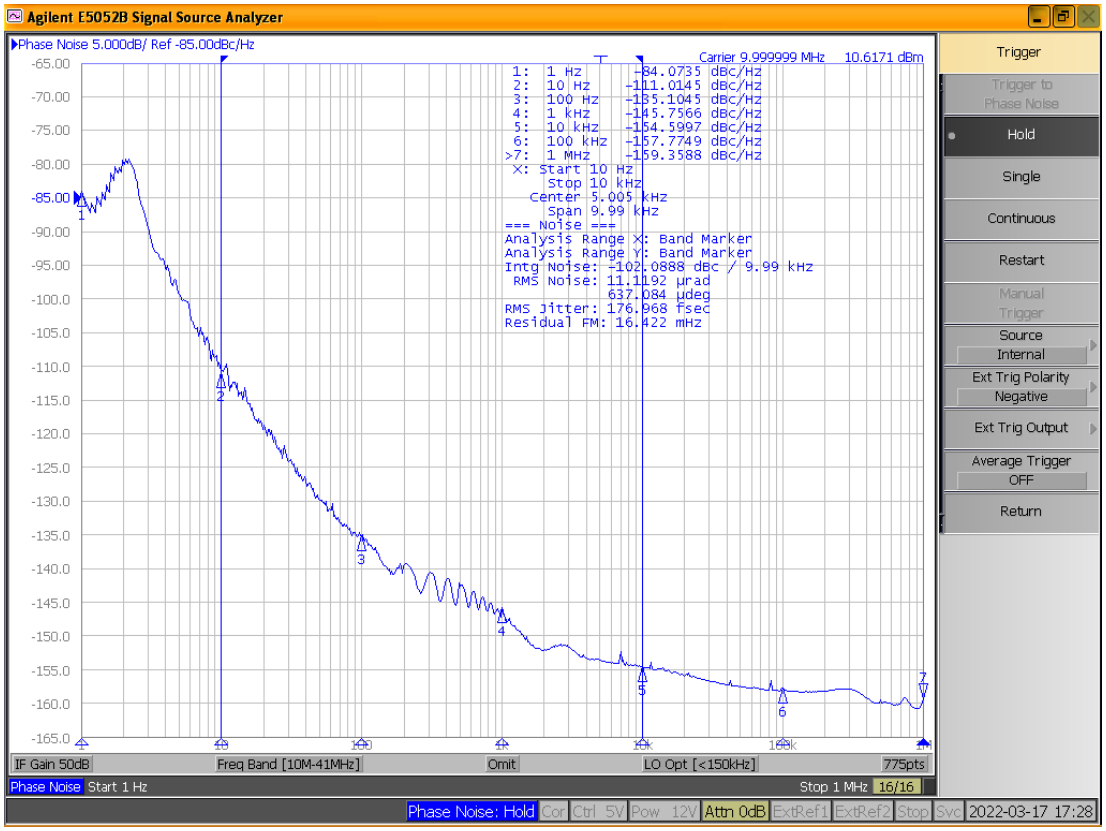

Figure 3.3 VCLK Phase Noise Data (GF-8803)

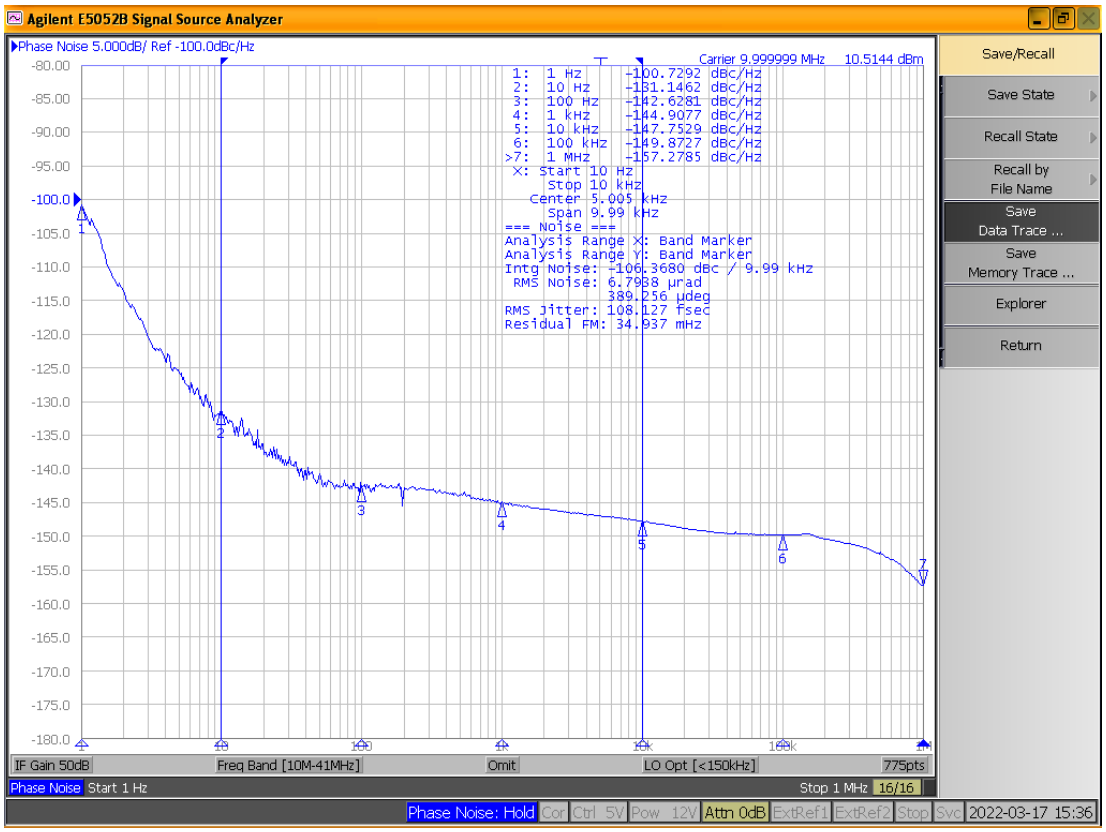

Figure 3.4 VCLK Phase Noise Data (GF-8804, GF-8805)

3.3 VCLK_SIN

Table 3.3 shows an overview of VCLK_SIN specifications. There is no single definition of frequency precision. The overall short term stability specifications of VCLK_SIN are defined in Table 3.3.

Table 3.3 VCLK_SIN Performance Specifications

Item		Receiver status	Unit	GF-880x series	
				8804	8805
Short term stability(1) (Root Allan deviation τ=1sec)		Fine Lock	-	±1E-11 (Max)-	
		Holdover			
Long term stability(1) (Average 24 hour)		Fine Lock	-	±1E-12 (Max)	
		Holdover	-	±1E-10 (Max)	±3E-11 (Max)
10MHz Phase noise	1Hz	Fine Lock	dBc/Hz	-90 (Max)	
	10Hz			-120 (Max)	
	100Hz			-135 (Max)	
	1kHz			-145 (Max)	
	>10kHz			-145 (Max)	
	1Hz	Holdover		-90 (Max)	
	10Hz			-120 (Max)	
	100Hz			-135 (Max)	
	1kHz			-145 (Max)	
	>10kHz			-145 (Max)	
Accumulating phase noise	10 to 10kHz	Fine Lock	dBc	-95 (Max)	
		Holdover			

-: Not Applicable

Notes:
(*1) Refer to Section 4.1 of the Hardware specifications for environmental conditions.

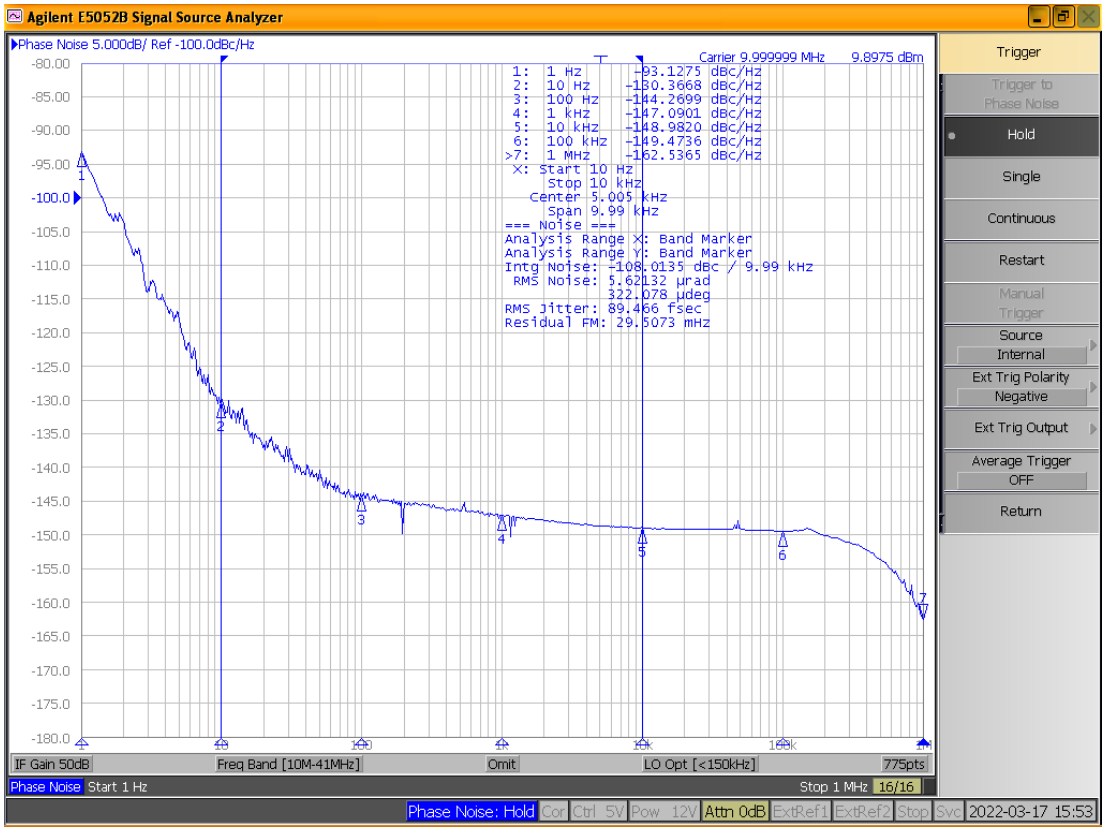

Figure 3.5 VCLK_SIN Phase Noise Data (GF-8804, GF-8805)

4 General Time Sequence

This chapter describes the general transition time chart and the main behavior of external event trigger.

4.1 Parameter Input Sequence

Figure 4.1 shows an overall response time using a command from the host side.

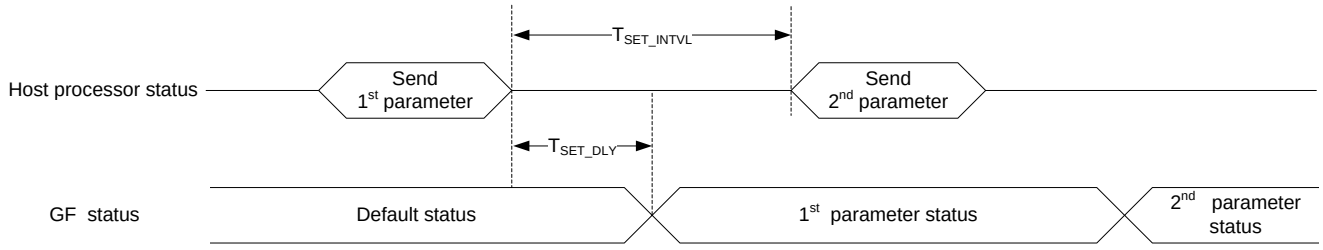

Figure 4.1 Parameter Input Sequence

Table 4.1 Parameter Input Sequence

Symbol	Description	Unit	Min	Typ	Max
T_{SET_DLY}	The response time after the host command is transmitted until the command is accepted by the internal operation.	second	–	–	2
T_{SET_INTVL}	The waiting time of the next command transmission after the previous command is sent.	second	–	–	0

4.2 Normal Operation

This section describes the relationship between the GNSS receiver status and the frequency mode without EPPS in a normal operation sequence. GNSSDO has the following two kinds of the relationship between the PPS reference status and the frequency mode based on the time difference between UTC decoding and Coarse Lock processing.

Case 1: Coarse Lock processing time is faster than UTC decoding time.
The frequency mode changes to Coarse Lock by synchronizing with GPS.

Case 2: UTC decoding time is faster than Coarse Lock processing time.
The frequency mode changes to Coarse Lock by synchronizing with UTC.

In this section, Case 1 is applied as normal time sequence.

4.2.1 Initial Power ON Sequence

Figure 4.2 shows the process time from completing Warm Up and position fixed after power on and until Fine Lock are achieved.

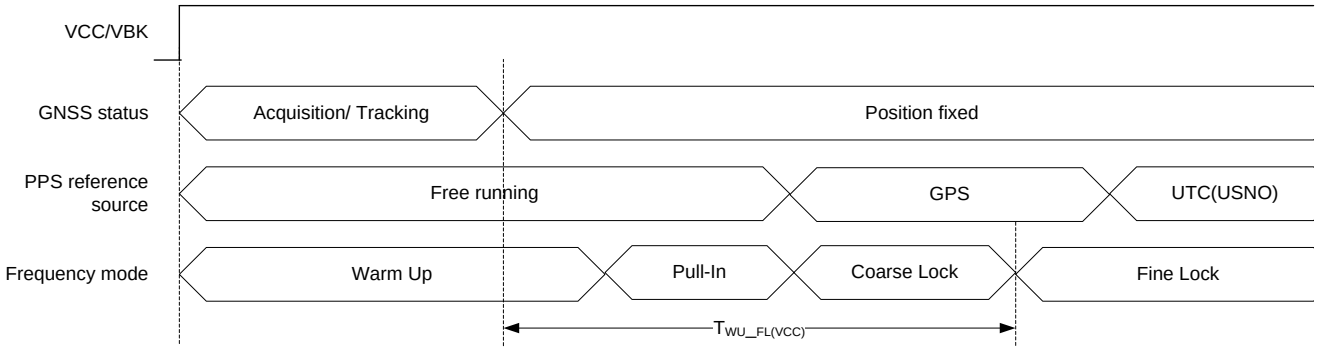

Figure 4.2 Initial Power ON Sequence

Table 4.2 Initial Power ON Sequence

Symbol	Description	Condition	Unit	Min	Typ	Max
$T_{WU\_FL(VCC)}$	The process time from position fixed until Fine Lock is achieved	Power on sequence	minute	–	–	5

4.2.2 Hardware External Reset Sequence

Figure 4.3 shows the process time from completing Warm Up and position fixed after an external hardware reset release and until Fine Lock is achieved.

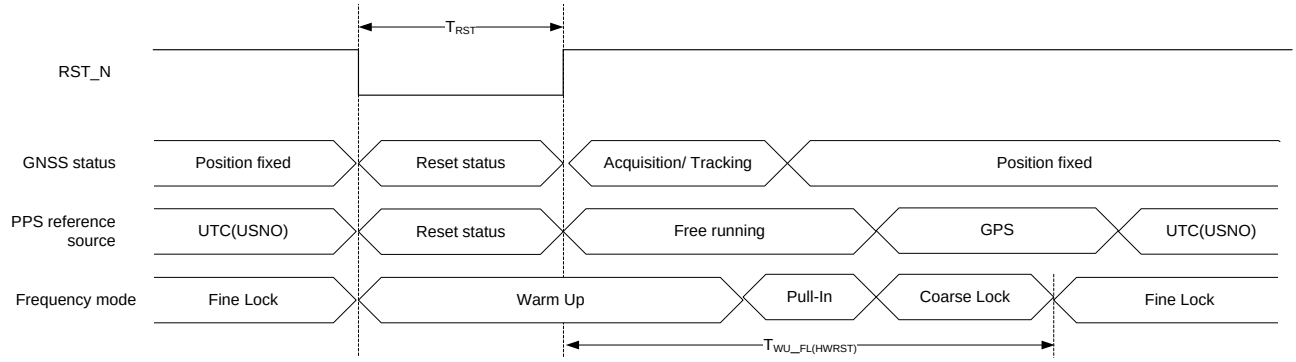

Figure 4.3 External Reset Sequence

Table 4.3 External Reset Sequence

Symbol	Description	Condition	Unit	Min	Typ	Max
$T_{WU\_FL(HWRST)}$	The process time from releasing external hardware reset until Fine Lock	External reset sequence by RST_N. Not dependent on reset time(T_{RST})	minute	–	–	5

4.2.3 Software Reset Sequence

Figure 4.4 shows the process time from completing Warm Up and position fixed after executing RESTART command and until Fine Lock is achieved.

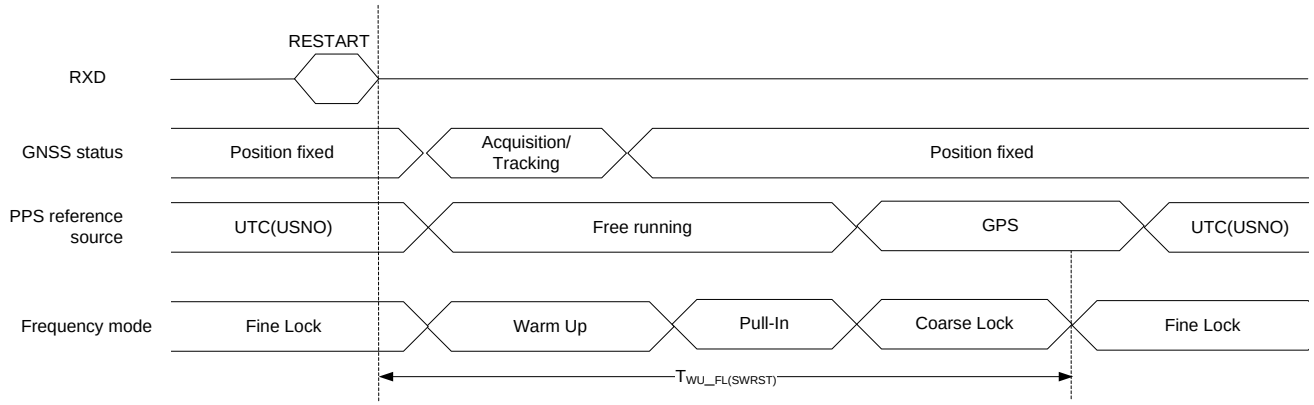

Figure 4.4 Restart Sequence with Power ON

Table 4.4 Restart Sequence with Power ON

Symbol	Description	Condition	Unit	Min	Typ	Max
$T_{WU\_FL(SWRST)}$	The process time from releasing external software reset until Fine Lock	External reset sequence by RESTART command	minute	–	–	5

4.2.4 Holdover Sequence

Figure 4.5 shows the process time after Holdover executed, from reacquisition of position fixed until Fine Lock achieved.

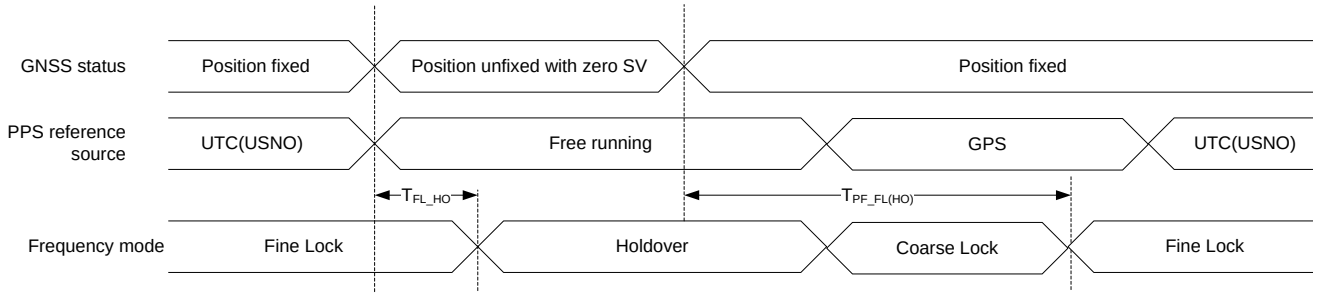

Figure 4.5 Holdover Sequence

Table 4.5 Holdover Sequence

Symbol	Description	Condition	Unit	Min	Typ	Max
T_{FL_HO}	The process time from Fine Lock until Holdover	Position unfixed	second	–	–	10
$T_{PF\_FL(HO)}$	The process time from position fixed until final Fine Lock	Holdover	minute	–	–	5

4.2.5 Out of Holdover Sequence

Figure 4.6 shows the process time after Out of Holdover executed, from reacquisition of position fixed until final Fine Lock.

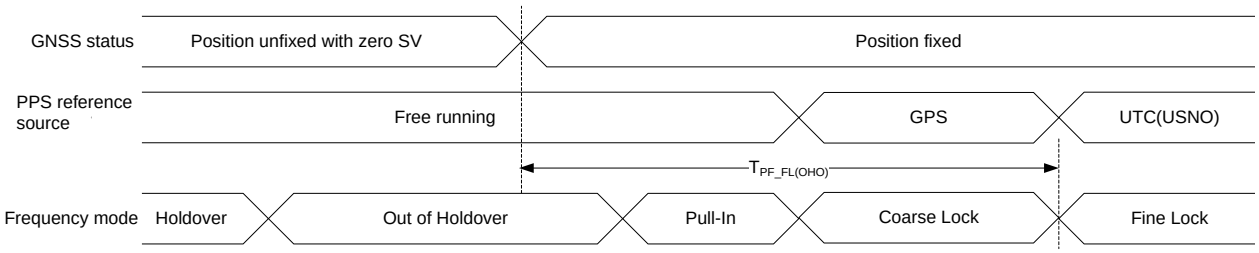

Figure 4.6 Out of Holdover Sequence

Table 4.6 Out of Holdover Sequence

Symbol	Description	Condition	Unit	Min	Typ	Max
$T_{PF\_CL(OHO)}$	The process time from position fixed until final Fine Lock	Out of Holdover	minute	–	–	5

5 Holdover Operation with HOSET

This chapter describes Holdover operation when using the HOSET command and CRZ (TPS4) status.
- HOSET command: learning time set and available time set
- CRZ (TPS4) status: learning time and available time

Table 5.1 shows the relationship between the frequency mode and the learning time/available time.

Table 5.1 Relationship between Frequency Mode and Control of Learning/Available Time

frequency mode	learning time	available time
Warm Up	Set to 0	Set to 0
Holdover		1 sec count down
Coarse Lock		
Fine Lock	Refer to Figure 5.1	
Out of Holdover	0 status	0 status

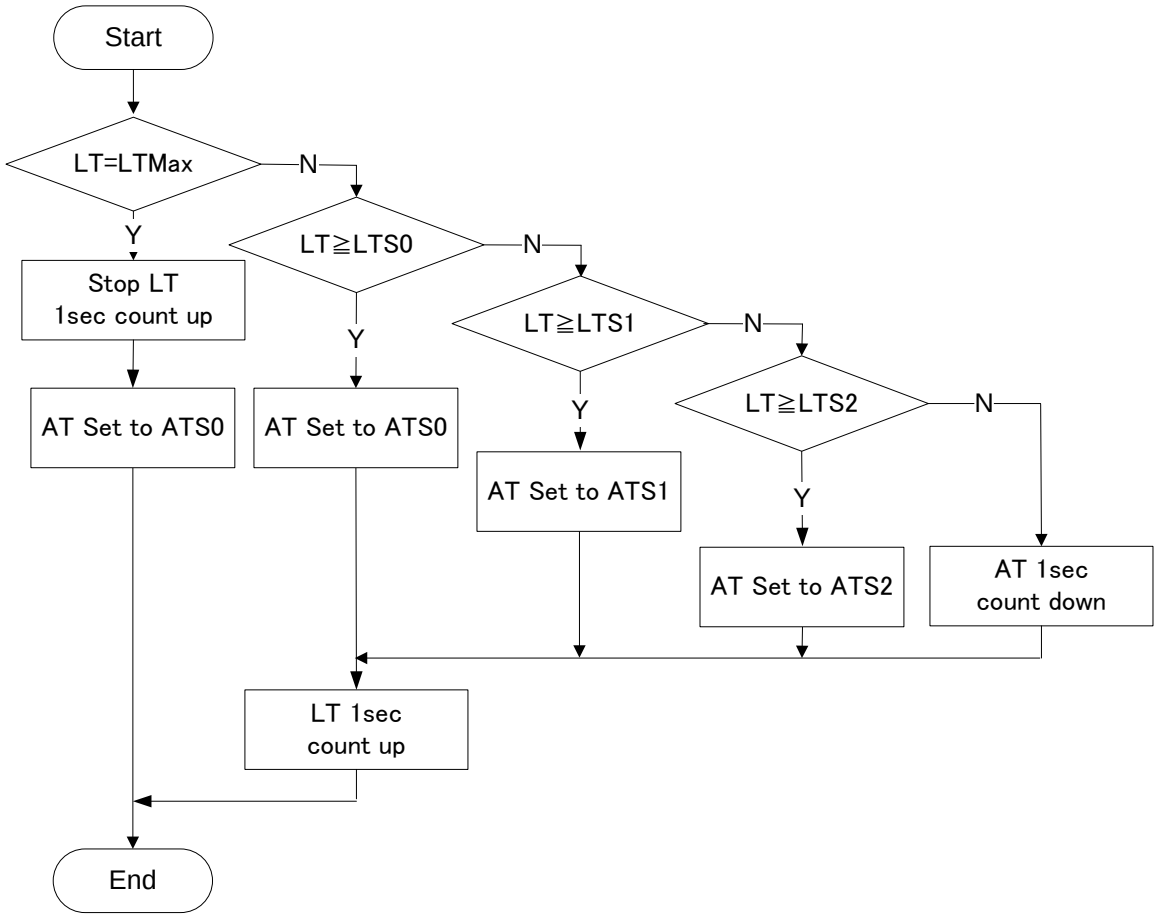

Figure 5.1 Relationship between Learning Time and Available Time in Fine Lock State

Here are the special messages in Figure 5.1.

LT: Current Learning time count data
LTMax: learning time set0 + 3600
LTS0: learning time set0 (HOSET Field 3)
LTS1: learning time set1 (HOSET Field 5)
LTS2: learning time set2 (HOSET Field 7)

AT: Available time count data
ATS0: available time set0 (HOSET Field 4)
ATS1: available time set1 (HOSET Field 6)
ATS2: available time set2 (HOSET Field 8)

Figure 5.2 shows an example based on the process of Table 5.1. The HOSET configuration is as follows:

Configuration condition: HOSET LTS2=ATS2=0. There is no LTS2 and ATS2 operation.

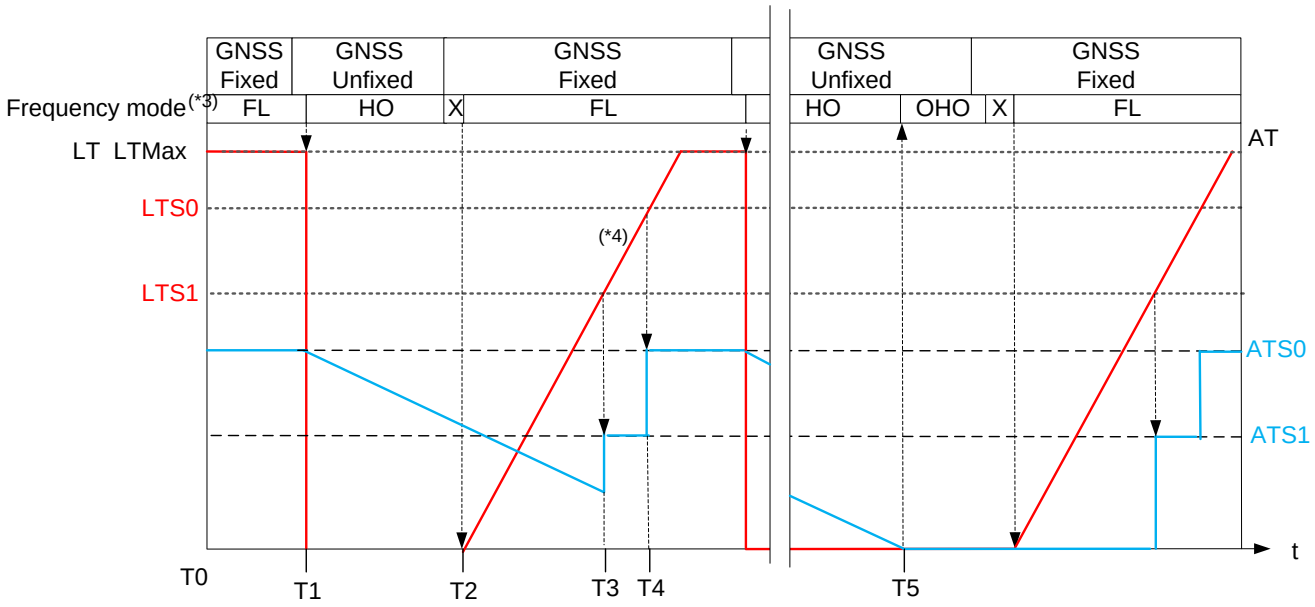

Figure 5.2 Relation of LT and AT to Frequency Mode

T0: Fine Lock is available 72 hours or more after power on of GNSSDO.
T1: Holdover start time - Sets learning time to zero. Starts the available time count down.
T2: Fine Lock start time - Starts learning time increment. Maintains available time count down.
T3: Available time set time - Sets available time to "available time set1" when the learning time equals "learning time set1".
T4: Available time set time - Sets available time to "available time set0" when learning time equals "learning time set0".
T5: Out of Holdover start time - Starts Out of Holdover after available time reached zero.

Notes:
(*3) Here are the special messages in Figure 5.2.
FL: Fine Lock (frequency mode is 3)
HO: Holdover (frequency mode is 4)
OHO: Out of Holdover (frequency mode is 5)
X: Pull-In or Coarse Lock (frequency mode is 1 or 2)
(*4) The decremental angle of available time is same as the incremental angle of learning time per unit of time. However in order to understand the behavior relationship between learning time and available time, both angles per unit of time are shown separately in this figure.

The GNSSDO guarantees 24 hours Holdover performance by continuously learning time for a 72 hours period. To guarantee the performance specifications the default Holdover control parameters are as follows:
-LTS0=72 hours
-ATS0=24 hours
-Others =0
If Holdover occurs before the learning time reaches the 72 hours default requirement, the frequency mode moves to Out of Holdover to avoid exceeding the 24 hours Holdover specification.

If the user application does not require the 24 hours Holdover time specification, the user can control Holdover time using LTS1, LTS2, ATS1 and ATS2 to meet their specific requirement. Please ensure the operation parameters (except LTS0 and ATS0) meet the required Holdover specifications. It is the user's responsibility regarding the Holdover performance. Figure 5.3 shows two examples of Holdover operation.

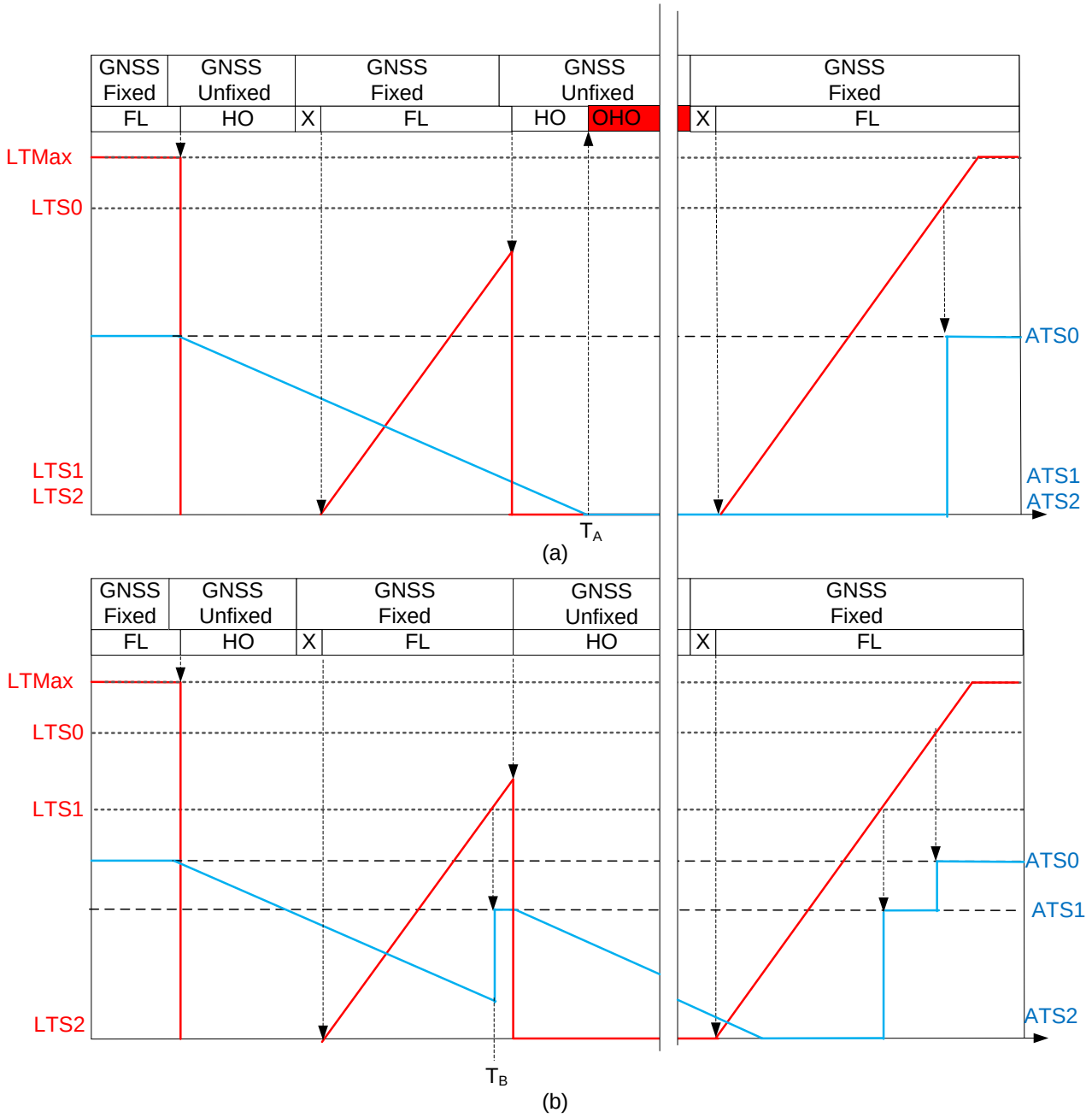

Figure 5.3 Relation Default to Customization by LTS1 and ATS1 about Holdover Process

Figure 5.3 (a) shows that the frequency mode moves to Out of Holdover at T_A after elapse of 72 hour default learning time and 24 hour Holdover becomes available.

Figure 5.3 (b) shows that the frequency mode does not move to Out of Holdover because the available time is set to ATS1 at T_B and the learning time is set to LTS1.Therefore since ATS1 initiates the reduction of AT at Holdover start time, the frequency mode does not move to Out of Holdover when the frequency mode moves to Fine Lock within ATS1.

6 Phase Skip Operation with PHASESKIP and MODESET

This chapter describes the relationship between PHASESKIP command and PPS behavior. Figure 6.1 shows the phase skip process at Pull-In mode is executed.

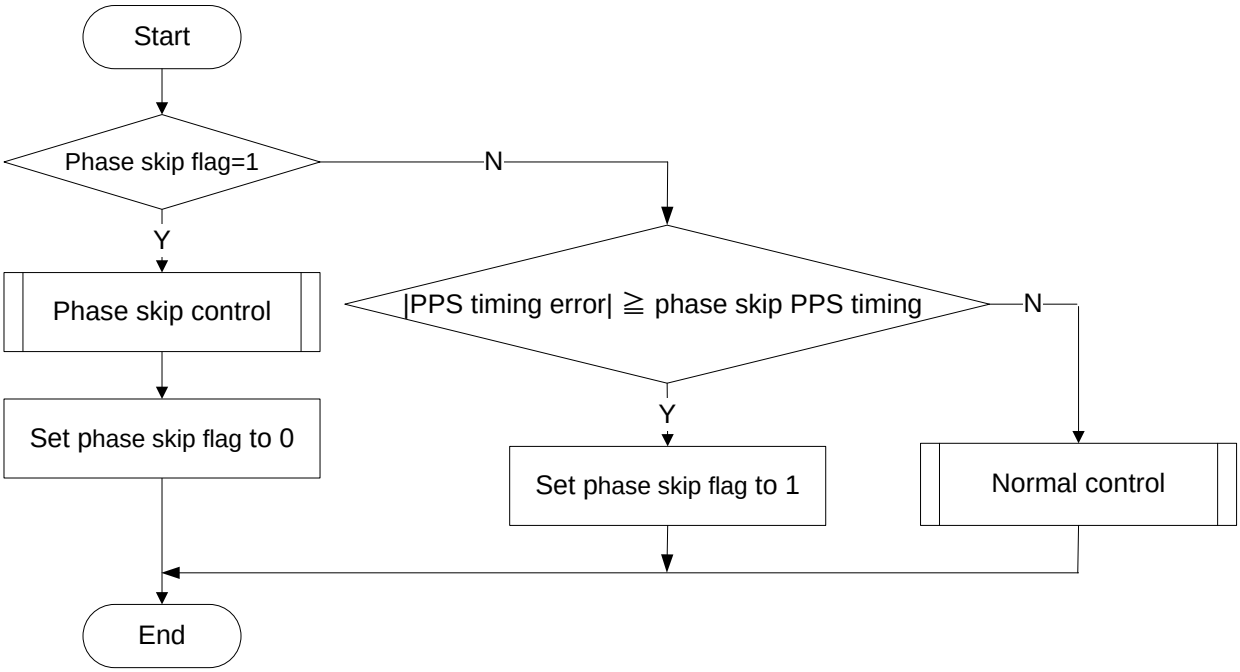

Figure 6.1 Phase Skip Operation Flow with PHASESKIP

The phase skip process is executed forcibly only when the frequency mode moves to Pull-In mode. If the user wants to execute the phase skip process again, the user should set the phase skip flag to 1.

Figure 6.2 shows the phase skip process with the following internal operation when the frequency mode moved to Pull-In mode at T_{PI}.

The Local PPS has a PPS timing error with the number of N 10MHz against Reference PPS. By executing phase skip process, the Local PPS reaches 10MHz which is nearest Reference PPS after one second.

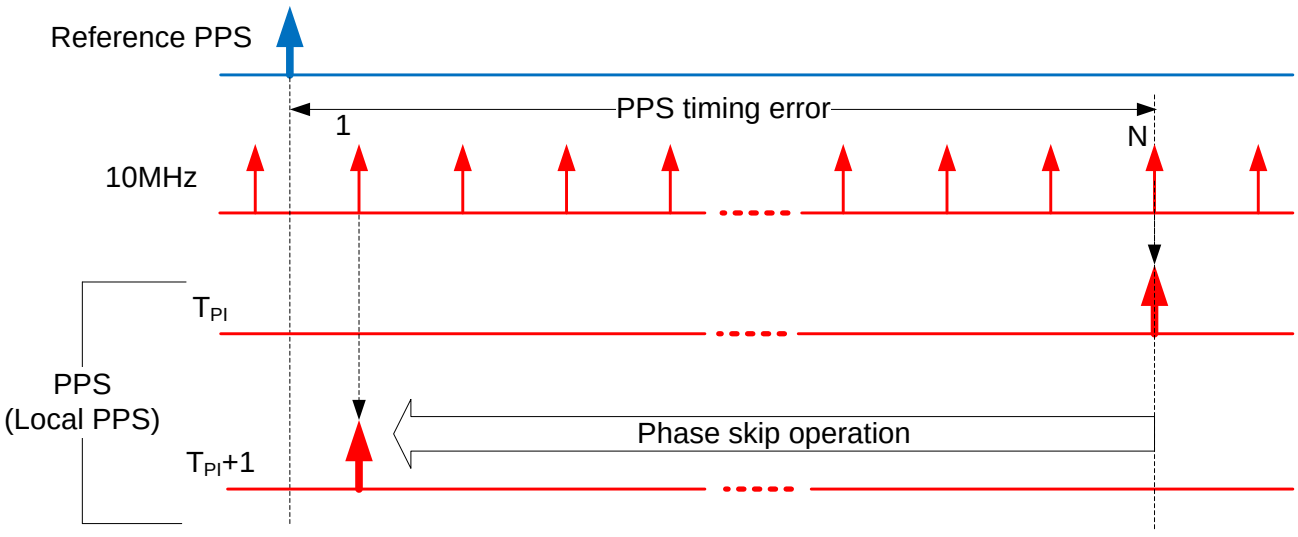

Figure 6.2 Relationship between Reference PPS and Local PPS with Phase Skip Process

7 Measurement Configuration Using Universal Frequency Counter 53132A

This chapter describes the measurement operations of PPS and VCLK using a 53132A (Keysight Technologies) that is a universal frequency counter. Figure 7.1 shows a measurement environment for measuring the PPS accuracy based on the Time Interval Counter mode of 53132A. Figure 7.2 shows a measurement environment for measuring the VCLK precision based on the Frequency Ratio mode of 53132A. Both measurements use a GPS Disciplined Rubidium Oscillator as the Time Base.

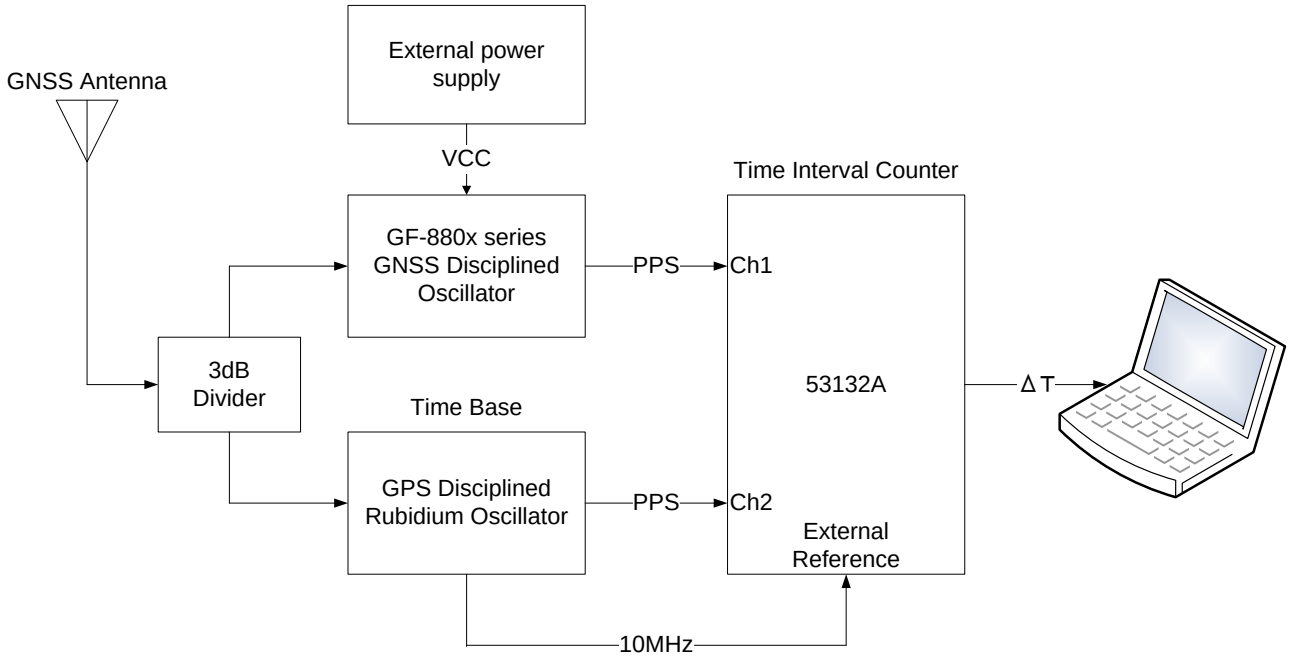

Figure 7.1 Measurement Environment of PPS Accuracy

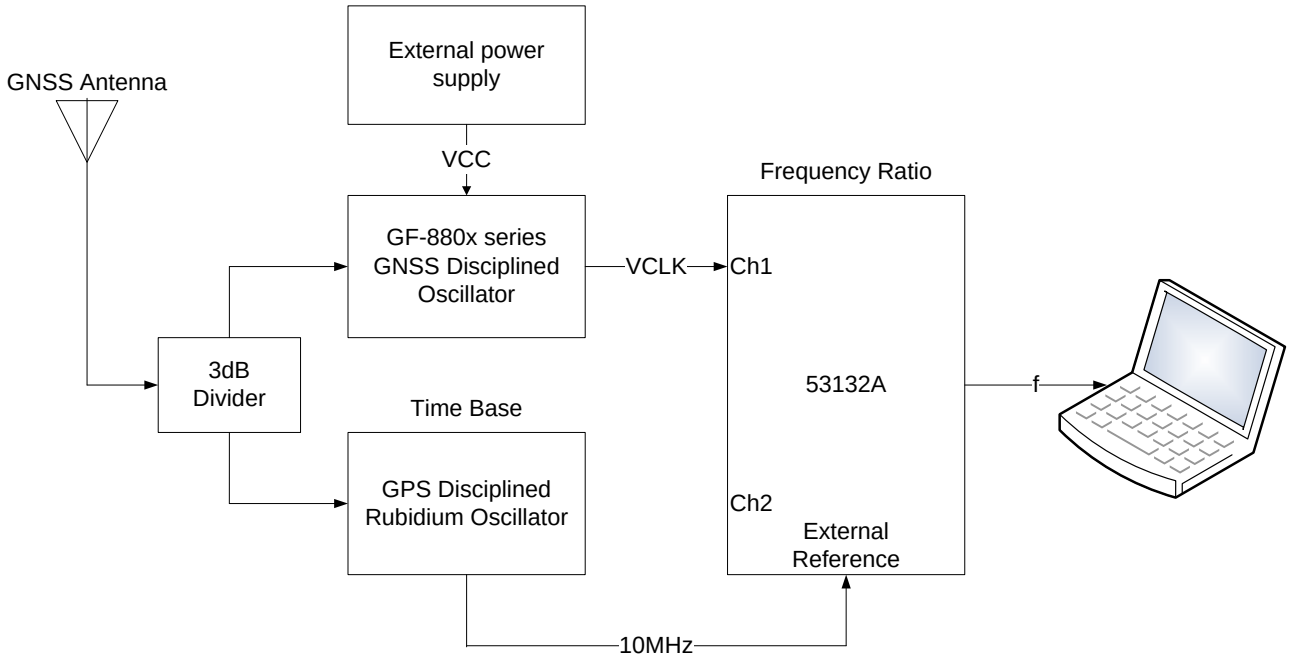

Figure 7.2 Measurement Environment of VCLK Precision

Figure 7.3 shows the simultaneously measurement data at room temperature of both PPS accuracy and VCLK precision at GF-8803 power on sequence. Figure 7.4 shows the Holdover characteristics after 72 hours learning time under 20°C dynamic temperature change condition of GF-8805 of which number of samples is ten.

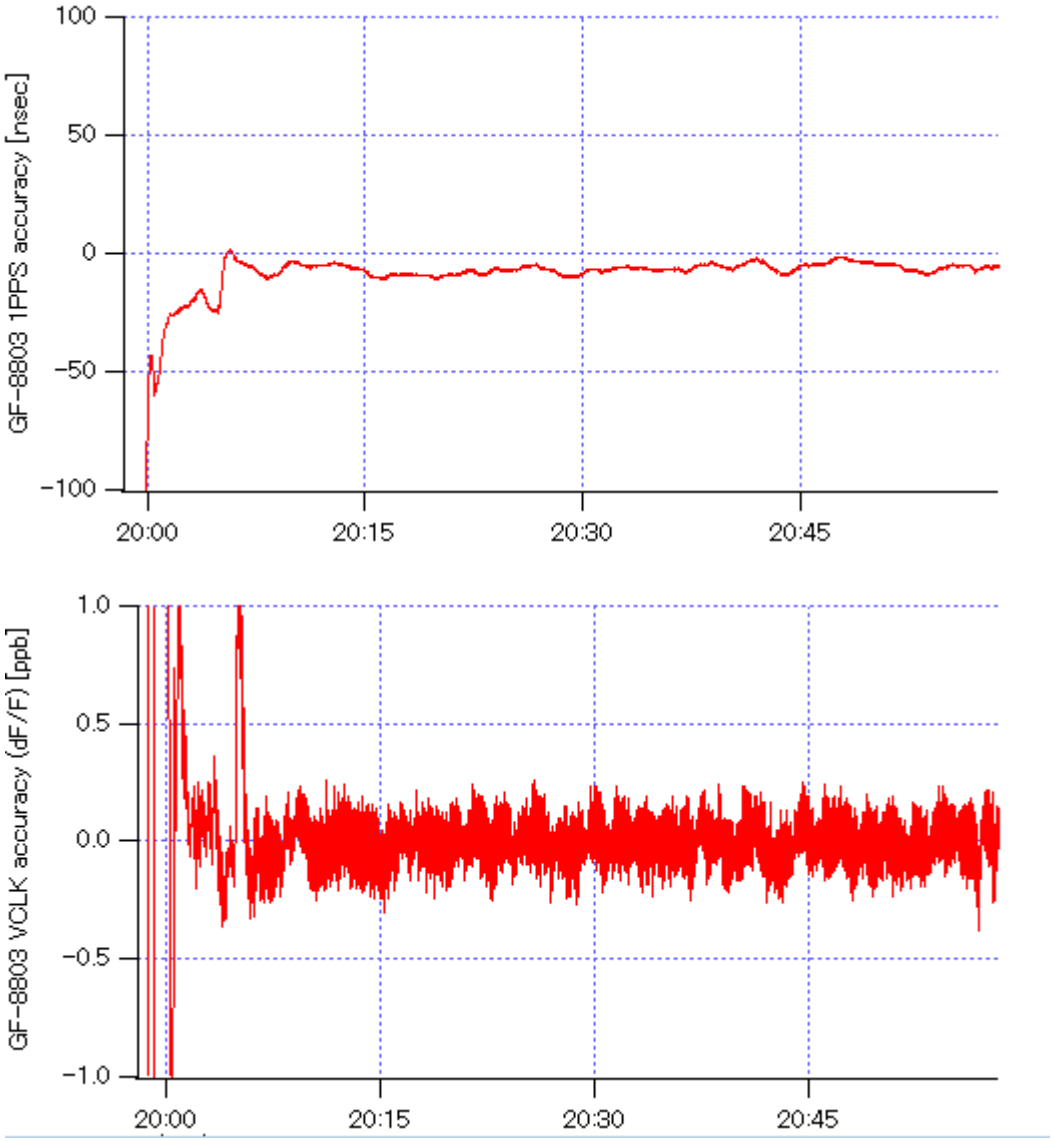

Figure 7.3 Measurement Data of PPS and VCLK Accuracy for GF-8803

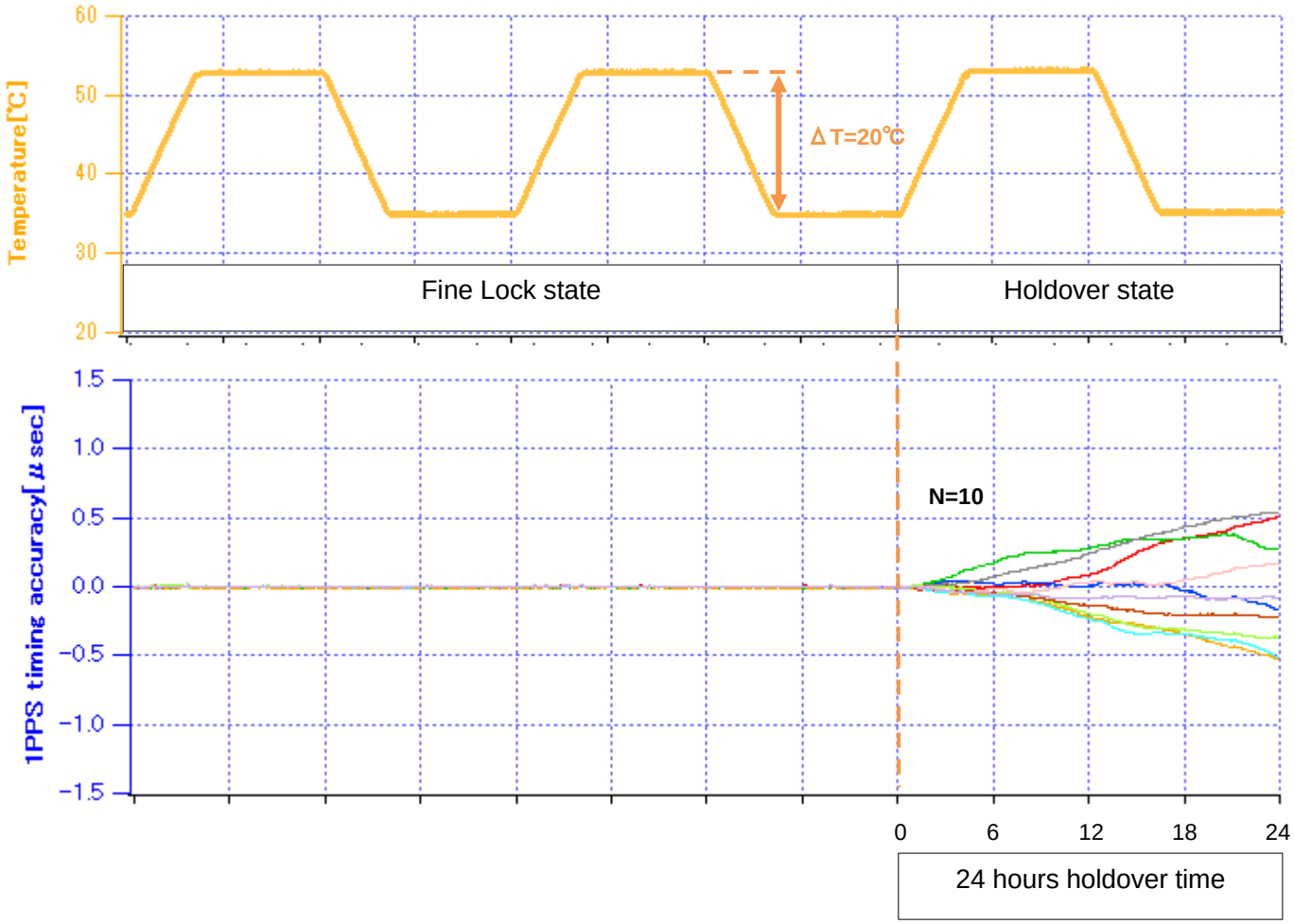

Figure 7.4 Measurement Data of PPS Holdover Characteristics for GF-8805

8 Antenna Configuration

This chapter describes the antenna interface function. Figure 8.1 shows the antenna configuration for the GNSSDO. The GNSSDO is able to stop over current condition with an internal threshold over current detection circuit. The antenna current shut down process triggers when the antenna detection circuit detects a shorted condition using a pre-determined current threshold. Figure 8.2 shows the antenna current status after shorted antenna condition has occurred.

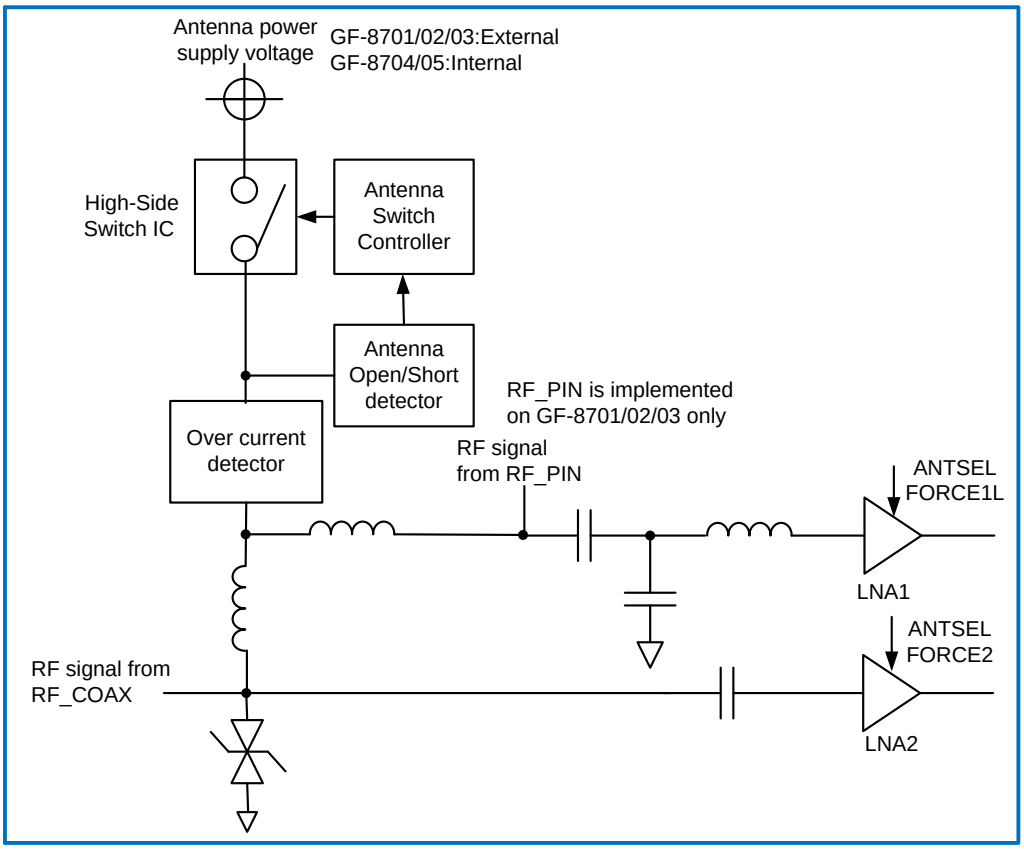

Figure 8.1 Antenna Configuration Diagram

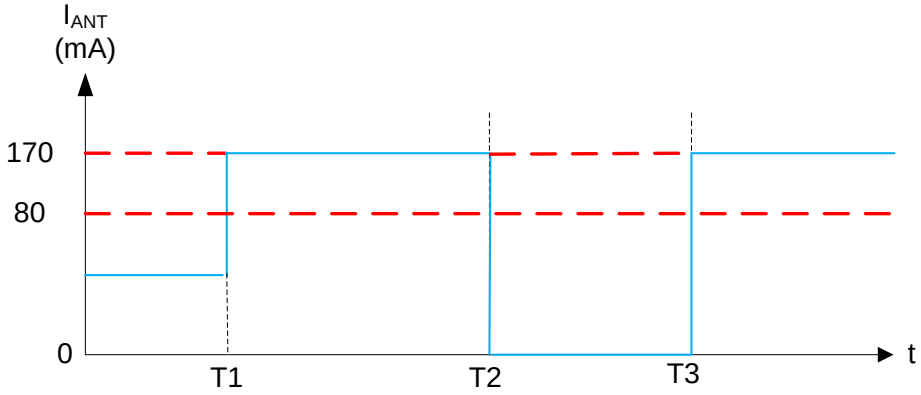

Figure 8.2 Antenna Current Control Configuration at Short Mode

T1: Over current process works by detecting antenna short condition.
T2: Antenna power supply voltage is shut down when circuit detects shorted condition of antenna.
T3: Antenna power supply voltage recovers and available after antenna short removed.